REMARKS

First, claims 11-20 (now new claims 21-40) are rejected under 35 U.S.C. § 112, first paragraph, for the reasons noted in the official action, wherein the Examiner specifically refers to a lack of support for storing device processes in the process devices and for process devices that indicate the completion of a device step to a master controller.

In response to the lack of support for storing device processes in the process devices, the Applicant refers the Examiner to the descriptions of Process Step Memories 16 in, for example, paragraphs 030, 036, 043, 044, 045, 049, 050, 058 and 059 of the specification and as shown, for example, in Figs. 1, 2A and 3. It is the belief and position of the Applicant that the pending application contains more than adequate support for storing device processes in process step memories in the process devices and respectfully requests that the Examiner reconsider and withdraw all rejections under 35 U.S.C. § 112, first paragraph.

In response with regard to the rejections under 35 U.S.C. § 112, first paragraph for a lack of support for process devices that indicate the completion of a device step to a master controller, the Applicant refers the Examiner to paragraphs 015, 017, 050, 053, 058 and 064 of the specification and to Fig. 3 and Step Complete 40 signal described and shown therein. It is the belief and position of the Applicant that the pending application contains more than adequate support for process devices that indicate the completion of a device step to a master controller, and respectfully requests that the Examiner reconsider and withdraw all rejections under 35 U.S.C. § 112, first paragraph.

Next, the Examiner rejects claims 2-4, 7-9 and 11-20 under 35 U.S.C. § 112, second paragraph, as being indefinite for the reasons noted in the official action. In response, the Applicant accordingly amends the rejected claims and the presently pending claims are now believed to particularly point out and distinctly claim the subject matter regarded as the invention, thereby overcoming all of the raised § 112, second paragraph, rejections. The entered claim amendments are directed solely at overcoming the raised indefiniteness rejection(s) and are not directed at distinguishing the present invention from the art of record

in this case and are fully support by the specification and drawings of the pending application as originally filed. In view of the foregoing, the Applicant respectfully requests that the Examiner reconsider and withdraw all rejections under 35 U.S.C. § 112, second paragraph.

Next considering the claim rejections and indications of allowable subject matter, the Examiner indicates that claim 13 would be allowable if amended to overcome the rejection under 35 U.S.C. § 112, second paragraph, and to include all limitations of the base claim and any intervening claims. The Applicant thanks the Examiner for indicating that claim 13 would be allowable and, in accordance with this indication, the claim 13 is appropriately revised and rewritten in independent form including all limitations of the base claim and any intervening claims and claim 13 is now believed to be allowable.

Next considering the rejections of claims over the cited prior art, the Examiner rejects claims 1, 4-6, 8, 10-12, 14-16, 18 and 20 under 35 U.S.C. § 102(b) over Shidara '444 and claims 1, 4-6, 11, 12 and 14-16 under 35 U.S.C. § 102(b) over Yellowley '017. The Applicant acknowledges and respectfully traverses all of the raised anticipatory rejections in view of the following remarks.

First considering the teachings of Shidara '444, this reference describes a control apparatus for a PLC system comprised of a main body control apparatus and a plurality of remote PLC devices wherein the main body apparatus and each remote PLC device includes a data processing/control processor, a program memory and a communications mechanism that bi-directionally interconnects the main body control apparatus and the remote PLC devices through a communications bus and wherein each remote PLC device may control an exterior device.

According to Shidara '444, there is a control program for the main body apparatus and a separate control program for each remote PLC device, with the programs being generated or stored in the main body apparatus and the remote PLC device programs being downloaded from the main body apparatus and to the individual remote PLC devices at system initialization. Further according to Shidara '444, the control exerted over the remote PLC devices by the main

body apparatus is limited to exchanges of data with the remote PLC devices and general management of the operations of the system. More specifically, the actions of the main body apparatus are limited to initialization of the system, including downloading of the individual PLC device programs to the remote PLC devices, the issuance of a start command for the remote PLC devices to begin execution of their respective remote PLC device programs and the issuance of a stop command to cease execution of the remote PLC device programs. Shidara '444 explicitly states that once the main body apparatus has issued a start command to one or more remote PLC devices, the individual remote PLC devices will repetitively execute their respective individual programs until receiving a stop command from the main body apparatus.

It is, therefore, seen that the present invention is distinguished over and from the teachings of Shidara '444 under the requirements and provisions of 35 U.S.C. § 103 for a number of fundamental reasons. For example, and as already stated by the Examiner with respect to claim 13 (now new claim 33), Shidara '444 does not teach, suggest or disclose a master controller generating a next step identifier to each device controller in response to each of the plurality of device controllers completing execution of a device step of their respective device processes.

In a related further distinction between the present invention and the teachings of Shidara '444, Shidara '444 teaches that each remote PLC device will independently and repetitively execute its individual remote PLC device program upon receiving a start command from the main body apparatus and will continue repeating the remote PLC device program until receiving a stop command from the main body apparatus. In fundamental contrast from the teachings of Shidara '444, the process devices and device controllers of the present invention will execute each successive device step only upon receiving a corresponding next step identifier from the master controller and will execute only the device step identified by the next step identifier.

In further basic distinction between the present invention and the teachings of Shidara '444, it must be noted that in the Shidara '444 system, each remote PLC device program is written separately and independently from the corresponding remote PLC device, such as in the main body apparatus or in a separate system, and is only downloaded to the remote PLC device.

In contrast, in the present invention each device step of each device process is created in the device controller of a process device from user provided control inputs directing the corresponding device controller and process device through each of the device steps, or operations, of the device process for that device controller and process device, and are stored directly in the process step memory of the device controller. Stated more simply, each device step of each device process is generated individually for the corresponding device controller and device process by a user directly directing the process device through the operations of the device process. It should be noted that in the present invention the device processes of each of the device controllers may be uploaded to the master controller for storage and subsequent reloading into the device controllers, but that the device processes are always generated in the device controllers individually and for each device controller.

According to the present invention, the device processes are generated by means of one or more input devices, each of which is associated with a particular process device and associated device controller at least during the creation of the device process for the particular process device and associated device controller. A single such input device may, for example, be connected to the master controller and associated with each process device and device controller, in turn through the system bus interconnecting the master controller and the device controllers, or may be directly connected to each individual device controller. Alternately, a plurality of input devices may be connected to the master controller and used concurrently with each input device being associated with one device controller at a time for the purpose of generating a device process for the process device associated with the device controller.

In either case, the input device or input devices may be assigned to successive device controllers if and as required.

In yet another implementation, there may be a plurality of input devices with each connected directly to a corresponding one of the device controllers to generate the device processes for the device controllers and the associated process devices. The input devices may be used concurrently to generate the device processes for a corresponding plurality of process devices and associated device controllers at a time, or one at a time to generate a device process for one process device and device controller at a time, and the input devices may be moved among the various device controllers as required.

In each of these implementations, however, and in fundamental contrast from the teachings of Shidara '444, the present invention follows the principle of generating a device process for a process device and the associated device controller, an storing it in the process step memory of the device controller, by means of an input device directly or indirectly associated with the process device and device controller. According to the present invention, any the input device is used by a user to generate process device control signals directly directing the process device and associated device controller through each operation of the device process, the control signals being stored in the process step memory of the device controller.

Next, referring to Yellowley '017, this reference describes a master control system for a multi-operation system comprised of a plurality of slave computers, each of which controls a microcontroller and includes a memory for storing a plurality of sequential movement instructions for directing operations of the associated microcontroller. The sequential movement instructions are executed in sequential steps according to coordinating pulses transmitted by a coordinating computer and the operations of each of the slave computers is terminated if any slave computer sets a flag indicating that a present movement by the associated microcontroller is not within predetermined tolerances of the current movement instruction of the sequential movement instructions provided for that slave computer.

It will be apparent that the present invention is distinguished over and from the teachings of Yellowley '017 under the requirements and provisions of 35 U.S.C. § 103 for essentially the same fundamental reasons discussed above with regard to Shidara '444.

For example, and as already stated by the Examiner with respect to claim 13 (now new claim 33), Yellowley '017 does not teach, suggest or disclose a master controller generating a next step identifier to each device controller in response to each of the plurality of device controllers completing execution of a device step of their respective device processes.

In related further distinction between the present invention and the teachings of Yellowley '017, Yellowley '017 teaches that each slave computer will execute its individual set of sequential movement instructions independently of and separately from both the master control system and the other slave computers. While the execution of each instruction will be synchronized with a clock signal transmitted by the master control system, whether a given instruction will be executed and which instruction will be executed are under the sole control of the slave computer and is independent of the execution of instructions by all other slave computers. The sole actual control over the execution of instructions by a slave computer, by either the master control system or other slave computers, is provided by a flag mechanism whereby the operations of each of the slave computers is terminated if any slave computer sets a flag indicating that a present movement by the associated microcontroller is not within predetermined tolerances of the current movement instruction.

In fundamental contrast from the teachings of Yellowley '017, the process devices and device controllers of the present invention will execute each successive device step only upon receiving a corresponding next step identifier from the master controller which, in turn, is dependent upon the device controllers providing a completed current step to the master controller, and each process device and device controller will execute only the device step identified by the next step identifier.

In further basic distinction between the present invention and the teachings of Yellowley '017, it must be noted that in the Yellowley '017 system, the sequence of movement

instructions for each slave computer is written separately and independently from the slave computers themselves and may, for example, be written in the master control system or in a separate system, and is only downloaded to the corresponding slave computer.

According to the present invention, and in basic contrast from the teachings of Yellowley '017, each device step of each device process is created in the device controller of a process device from user control inputs entered through an input device associated with the process device and directing the corresponding device controller and process device through each of the device steps, or operations, of the device process for that process device, with each device step being stored directly in the process step memory of the device controller. Stated more simply, each device step of each device process is generated individually for the corresponding device controller and device process by a user directly directing the process device through the operations of the device process.

It is the belief and position of the Applicant that the present invention, as recited in the claims as amended herein, are fully and patentable distinguished over and from the teachings and suggestions of both Shidara '444 and/or Yellowley '017 under the requirements and provisions of 35 U.S.C. § 103 and for the reasons discussed herein above. Further in this regard, it will be noted that the Applicant amended independent claims 1 and 11 as well as claim 13 (now new claims 21, 31 and 33, respectively), so that each independent claim recites at least one of the distinctions over both Shidara '444 and Yellowley '017 that have been discussed herein above, thereby allowing claims 1 and 11 as well as claim 13 (now new claims 21, 31 and 33, respectively), to distinguish over the prior art under the requirements and provisions of 35 U.S.C. § 103.

In particular, claim 13 is rewritten as new claim 33 in accordance with the Examiner's suggestion to recite the distinction over the prior art that of a master controller generating a next step identifier to each device controller in response to each of the plurality of device controllers completing execution of a device step of their respective device processes.

Further in this regard, the Applicant notes that there are a number of questions, objections and rejections that involve the master controller and the functions of the master controller, either directly or indirectly. Considering that further clarification of the recitations pertaining to the master controller may be beneficial in more clearly and explicitly defining the master controller and the functions of the master controller and the distinctions of the present invention over the cited prior art. For this reason, the Applicant has elected to amend the claim recitations to more explicitly define the master controller and the functions of the master controller in each instance wherein such amendments may directly or indirectly assist in more clearly defining the master controller.

In particular, the claims now explicitly recite that during the execution of a device process, the only function performed by the master controller is the generation of step execute identifiers to the device controllers. The changes in the wording of the claims thereby explicitly limit the role of the master controller during the execution of a device process to the issuing of successive step execute commands at appropriate times, thereby clearly defining the master controller as not operating as a master central processor or controller operating to control the actual execution of processes. Stated another way, during the execution of a device process the sole role of the master controller is to synchronize the starts of each of the successive process steps executed by the device controllers by issuing step execute commands at the appropriate times. The master controller therefore has no other functions during the execution of a device process.

Lastly in this regard, it must be noted that these amendments in the claims do not add any new subject patter to the claims or specification, and do not alter the scope of the invention as recited in the claims, but are presently solely to clarify certain recitations.

The Applicant elected to amend claims 1 and 11 (now new claims 21 and 31, respectively) to recite the distinguishing limitation that each device step of each device process is created in the device controller of a process device from user control inputs entered through an input device associated with the process device and directing the corresponding device

controller and process device through each of the device steps, or operations, of the device process for that process device, with each device step being stored directly in the process step memory of the device controller.

Finally, it must also be noted that the amendments and recitations of claims 1, 11 and 13 (now new claims 21, 31 and 33, respectively) are incorporated into the recitations of the dependent claims through dependency from one of claims 1, 11 or 13, so that the dependent claims are likewise distinguished and allowable over both Shidara '444 and Yellowley '017 under the provisions and requirements of 35 U.S.C. 103.

The Applicant respectfully requests that the Examiner reconsider and withdraw all rejections of the claims under 35 U.S.C. § 103 over the teachings and suggestions of either or both Shidara '444 and/or Yellowley '017 and allow the presently claims as amended herein.

If any further amendment to this application is believed necessary to advance prosecution and place this case in allowable form, the Examiner is courteously solicited to contact the undersigned representative of the Applicant to discuss the same.

In view of the above amendments and remarks, it is respectfully submitted that all of the raised rejections should be withdrawn at this time. If the Examiner disagrees with the Applicant's view concerning the withdrawal of the outstanding rejections or applicability of the Shidara '444 and/or Yellowley '017 references, the Applicant respectfully requests the Examiner to indicate the specific passage or passages, or the drawing or drawings, which contain the necessary teaching, suggestion and/or disclosure required by case law. As such teaching, suggestion and/or disclosure is not present in the applied references, the raised rejection should be withdrawn at this time. Alternatively, if the Examiner is relying on his/her expertise in this field, the Applicant respectfully requests the Examiner to enter an affidavit substantiating the Examiner's position so that suitable contradictory evidence can be entered in this case by the Applicant.

In view of the foregoing, it is respectfully submitted that the raised rejection(s) should be withdrawn and this application is now placed in a condition for allowance. Action to that end, in the form of an early Notice of Allowance, is courteously solicited by the Applicant at this time.

The Applicant respectfully requests that any outstanding objection(s) or requirement(s), as to the form of this application, be held in abeyance until allowable subject matter is indicated for this case.

In the event that there are any fee deficiencies or additional fees are payable, please charge the same or credit any overpayment to our Deposit Account (Account No. 04-0213).

Respectfully submitted,

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